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**Declaration of Timothy K. Carns**

**Document A**

# D1549 CAPACITOR LOT REPORT TDC37223

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## Executive Summary:

Lot D1549 was processed using the runcard attached in Appendix A on the Z37223 process flow. Previous analysis of lot D1114 indicated that the undercut of the capacitor poly by the interpoly dielectric (IPD) etch was causing a leakage path from the top plate to the bottom plate of the capacitor through the PEARL.

**Objective:** The objective of this experiment was to determine if the undercut of the top poly plate was the cause of capacitor leakage.

To evaluate the effect of these splits on rolloff.

To achieve a Cpk > 1.33 for all capacitor parameters.

This experiment used hook wafers to lot D1114 and experimental wafers to determine if the leakage could be reduced by not undercutting the poly 2. The hook wafers had the IPD oxide removed at L39 using a BOE etch. The experimental wafers had the IPD oxide removed at L40 etch prior to etching poly 1. Figures 1 and 2 show the resulting capacitor structures for the L39 etch and L40 etch respectively. The objective of the experiment was achieved because the capacitor which had PEARL touching both the poly 2 and the poly 1 showed significantly higher leakage than the capacitor which did not. This experiment did not answer if the leakage path is present only when PEARL is in-between the poly 2 and poly 1 or when PEARL is touching poly 2 and poly 1. Further experiments are planned to determine this answer. This will be done by using a spacer oxide technique which may seal off the side of the capacitor prior to PEARL deposition and/or by using a dry etch to remove the IPD oxide at L39 etch thereby preventing an undercut of the poly 2. Also the addition of IPD oxide under the PEARL causes an increase in LEFF variation that requires the IPD to be removed prior depositing the PEARL.

**Table 1 Post metal 1 Peval data from lot d1549 for the wafers which received a deposited oxide and the IPD oxide etched at L40 (wafers 8 – 10, 16 – 20, 23 – 25). The data from two sites on wafer 18 was not included in these statistics due to the oxide being blown.**

| Parameters        | Units               | Spec Min | Spec Mean | Spec Max | Data Mean | Data Sigma | Cp    | Cpk    |
|-------------------|---------------------|----------|-----------|----------|-----------|------------|-------|--------|
| CVCAN             | PPM/V               | -50      | 0         | 50       | -16.79    | 2.542      | 6.56  | 4.35   |
| CVCAP             | PPM/V               | -50      | 0         | 50       | -26.41    | 3.36       | 4.96  | 2.34   |
| IPOCAP            | fF/ $\mu\text{m}^2$ | 0.81     | 0.92      | 1.06     | 0.899     | 0.0063     | 6.61  | 4.71   |
| TOX electrical    | Å                   | 325      | 375       | 425      | 382.14    | 2.68       | 6.22  | 5.33   |
| BV                | Volts               | 8.0      | --        | --       | >25.0     | --         | >1.33 | >1.33  |
| CMAT              | %                   | -0.01    | 0         | 0.01     | -0.015    | 0.035      | 0.095 | -0.048 |
| Leakage @+5 Volts | fA/ $\mu\text{m}^2$ | --       | --        | 15.0     | 0.188     | 0.150      | 16.67 | 32.92  |
| Leakage @-5 Volts | fA/ $\mu\text{m}^2$ | --       | --        | 15.0     | 0.25      | 0.17       | 14.71 | 28.92  |

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**Table 5 Rolloff points for each split for BVDSS and IOFF. Process key: WA=no waffle etch compensation, NW=waffle etch compensation.**

| PROCESS        | BVDNROLL | IOFFNROLL | BVDPROLL | IOFFPROLL |
|----------------|----------|-----------|----------|-----------|
| Thermal_BOE_WA | 0.31     | 0.31      | <0.33    | 0.32      |
| Thermal_BOE_NW | 0.33     | < 0.33    | <0.35    | <0.35     |
| Thermal_BOE_NW | 0.34     | 0.35      | 0.36     | 0.36      |
| Dep_BOE_WA     | 0.30     | 0.30      | <0.34    | 0.34      |
| Dep_BOE_NW     | 0.30     | 0.30      | 0.33     | 0.34      |
| Dep_L40_NW     | 0.31     | 0.31      | 0.34     | 0.35      |

### **Conclusions and Recommendations:**

- The experiment done on lot D1549 has shown that the capacitor leakage can be minimized to within PSC spec values by etching the capacitor oxide at L40 instead of L39. The data suggests this is accomplished by not allowing PEARL to contact both poly 1 and poly 2 or by not allowing, the PEARL to get in-between the poly plates in the undercut region.
- The deposited oxides showed significantly fewer oxide failures than the thermal oxides. It is recommended that a QBD test be implemented for capacitor lifetime measurements.
- All parameters on the experimental group met their PSC specification limits, except for CMAT. Work on the other capacitors is required to resolve the issue with CMAT.
- Data from lot E0034 is required to determine if a process that does not have PEARL in-between the poly plates, and does not have capacitor oxide under the PEARL to minimize LEFF variation, can be achieved.
- The end of line Peval data should be used to do a detailed rolloff analysis as the post metal 1 data shows the thermal oxides to have higher rolloff values than the deposited oxides.
- An end of line Peval summary of the capacitor parameters is required to quantify any shifts in the capacitors from metal 1 to finished process.
- Implement deposited oxide due to improved capacitor and transistor rolloff results.

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OP 16

CONTROL NUMBER

28224

(DOC. CTRL.)

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## CHANGE NOTICE

☒ PERMANENT ☐ TEMPORARY (EXPIRES \_\_\_\_\_)EFFECTIVITY: ASAP

|                        |  |                   |               |            |              |
|------------------------|--|-------------------|---------------|------------|--------------|
| ORIGINATOR<br>DeBruler | RESPONSIBLE PERSON<br>Tim Carns<br><i>file 1-13-99</i> | DATE<br>1/11/1999 | DEPT #<br>633 | M/S<br>NB2 | EXT.<br>6917 |
|------------------------|--|-------------------|---------------|------------|--------------|

| TITLE                          | AFFECTED DOCUMENT | OLD REV | NEW REV |
|--------------------------------|-------------------|---------|---------|
| TECHNOLOGY DEVELOPMENT: Z37223 | TDC37223          | 22      | 23      |
|                                |                   |         |         |

D1549 CAPACITOR LOT REPORT

REASON  
FOR  
CHANGE☐ MAJOR☒ MINOR

## DESCRIPTION OF CHANGE

ADD FOLLOWING DOCUMENT

*2/2/99**16  
Converted to Design Library*

## APPROVALS

JOHN SMYTHE

*[Signature]*

DATE: 2-5-99

RICK WHITE

*[Signature]*

DATE: 2/23/99

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